Kurz-Kasch, Inc.
Electronics Division
1501 Webster Street
Dayton, Ohio 45404
Telephone (513) 223-8161

Operating Instructions For Model LP-610 & LP-620

DESCRIPTION

The Kurz-Kasch Logic Probes are designed for fast servicing and checking of integrated logic systems. With their unique multi-lamp readouts at the tips of the probes, the Logic Probes visually display the presence of correct logic levels by illumination of colored readouts marked "1" and "0". Incorrect logic levels are shown by the absence of illumination at the colored readouts.

Various optional features, described in later paragraphs, are available to significantly increase the versatility of the Logic Probes.

GENERAL SPECIFICATIONS

	Probe Series	
1. Operating Power	LP-610	LP-620
Vcc	4.75 to 5.5 Vdc	12 to 15 Vdc
Standby Current	60 MA	40MA
Current for each Readout	60 MA	55 MA
2. Nominal Logic Voltage Response		
Logic "0" illumination (White)	0 to .8 V	0 to 1.5 V
"Gray Area" (No illumination)	.8 to 2.4 V	1.5 to 10 V
Logic "1" illumination (Red)	2.4 to Vcc	10 V to Vcc
3. Input Impedance		
Minimum at either Logic Level	— Greater than 50K ohms —	
4. Overvoltage Protection	± 140 VDC	
At Probe Tip	110 VAC	
5. Power Lead Protection		
Maximum Reverse Current	0 MA	0 MA
Maximum Voltage	± 140 VDC	± 140 VDC

PULSE DETECTION

In the LP-610 and LP-620 series, a third readout (colored blue and marked "P") is provided in the probe tip and is illuminated for 200 milliseconds whenever a 30 nanosecond (or greater) pulse (or a pulse train) appears at the probe tip.

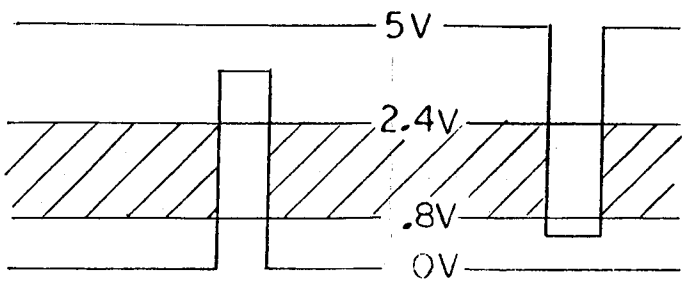

FIG. A

You must cross both thresholds to cause the pulse lamp to illuminate. Refer to Figure A above. The obvious benefit to you, the pulse must be of a VALID logic level in order for the pulse lamp to illuminate. No longer can glitches or small pulses or noise cause the pulse lamp to illuminate. Only VALID pulses will properly operate your logic and cause the pulse lamp to illuminate.

Cont'd.

MEMORY/STRETCH OPTION *(Probes with Suffix Letter "M")*

The slide switch near the rear of the "M" probes permits pulse detection in either "stretch" or "memory" modes. In the "stretch" mode (switch off) the blue "P" indicator illuminates for 200 milliseconds in response to each single pulse (positive or negative going) of 30 nanoseconds, or greater, duration. In the "memory" mode (switch slid to mem. position) the "P" indicator is illuminated indefinately after the first pulse or logic transition, until reset by sliding the switch to Off. To us the "memory" mode, first slide the switch to off, then connect the probe tip to the point being examined. This initial contact will cause the "P" indicator to flash. Following the initial "P" flash, the switch should be slid to mem. position. Now the probe is ready to operate in the "memory" mode.

5.0 NANOSECOND PULSE CAPABILITY OPTION *(Probes With Suffix Letter "S")*

Probes with this option have a pulse detection capability significantly faster than standard probes, in that a 5 nanosecond (or greater) pulse will illuminate the blue "P" indicator. Therefore, in these instructions, any 30 nanosecond limitation on pulse detection capabilities may be reduced to 5 nanoseconds for "S" probes.

3-CHANNEL INPUT OPTION *(Probes With Suffix Letter "G")*

Probes with the "G" option closely simulate a 2-input oscilloscope, in that two inputs are provided, and the blue "P" indicator will illuminate only when the gate input(s) are in coincidence. When only one gate input is used, the other should be connected to Vcc or left open (implied "1") and not grounded.

"G" OPTION PROBES ARE PROVIDED WITH A PLUG IN ASSEMBLY HAVING THE FOLLOWING ADDITIONAL LEADS:

Black Wire-Ground Although this lead is common with the black power lead it should be terminated at a ground point next to where the measurement is being taken. This is necessary for minimizing time delay.

Red Wire-Enable This lead must be connected to Vcc to enable the gating function. (Pulse lamp will be illuminated). Pulse lamp will remain illuminated only if white leads are in coincidence.

White Wire-Gate Inputs The maximum input at either of these leads should not exceed +5.5 VDC. Each input equals 1 - TTL load.

TO CHECK PROBE

1. Connect black power lead to ground.
2. Connect red power lead to + Vcc.
3. Touch probe tip to + Vcc, and red "1" readout should be illuminated.
4. Touch probe tip to − Vcc, and white "0" readout should be illuminated.

OPERATION OF THE PROBE

The red "1" readout will remain illuminated only during the time period when logic level "1" is present at the probe tip. Similarly, the white "0" readout will remain illuminated only during the time period when logic level "0" is present at the probe tip. The blue "P" readout will illuminate as the result of a transition in logic levels. Therefore, typical operating situations likely to be encounterd are as follows:

1. With probe tip touching symmetrical clock source, white and red indicators will both be illuminated at one-half brilliance, and blue "P" indicator will be illuminated at full brilliance.

2. With probe tip touching positive-going high-speed pulses of short duty cycle, white "0" and blue "P" indicators will be illuminated, red "1" indicator will be illuminated on duty cycles greater than 10%. An indication of symmetry can be obtained from the relative brilliance of the "0" and "1" indicators.

3. With probe tip touching negative-going high-speed pulses of short duty cycle, red "1" and blue "P" indicators will be illuminated, white "0" indicator will be illuminated on duty cycles greater than 10%. An indication of symmetry can be obtained from the relative brilliance of the "0" and "1" indicators.

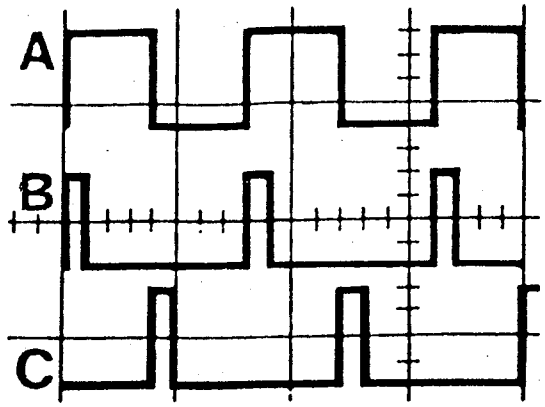

FIGURE 1

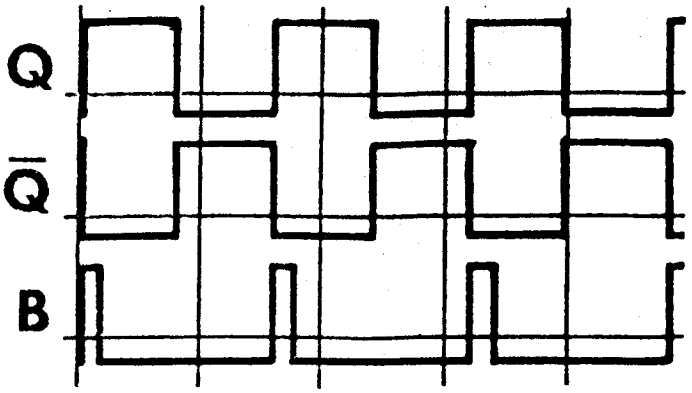

FIGURE 2

TYPICAL OPERATION OF THE GATING FEATURE *(Probes With Suffix Letter "G")*

A. Connect the red enable lead to Vcc. The blue "P" lamp will now be illuminated.

B. Connecting either white gating lead to ground must turn off pulse lamp.

C. In Figure 1 above, "A" is the input to one of the white gating leads.

D. If "B" is the input to the other white gating lead, the blue "P" lamp will be illuminated indicating coincidence.

E. If "C" is the input to the other white gating lead, the blue "P" lamp will not be illuminated indicating non-coincidence.

USE OF THE GATING FEATURE TO VERIFY TIMING RELATIONS *(Probes With Suffix Letter "G")*

A. Figure 2 represents a typical digital system with square wave as flip-flop output "Q" and "$\overline{Q}$". "B" is generated each time "Q" goes positive. This relationship may be verified by connecting one input gate (white wire) to flip-flop "Q" and using the second input gate (other white wire) at "B" as follows:

1. Connect one white gate lead to "Q" on flip-flop.
2. Connect other white gate lead to "B" in circuit.
3. Blue "P" indicator will be illuminated verifying that during the time "Q" and "B" are positive the two pulse trains are in coincidence.
4. Reconnect the gate lead that was connected to "Q" in step 1 on previous page to "$\overline{Q}$" and repeat step 2.
5. The blue "P" indicator will not be illuminated verifying that "B" is not generated during the time "$\overline{Q}$" is positive or non-coincidence.

USE OF THE GATING FEATURE IN PHASE TESTS *(Probes With Suffix Letter "G")*

1. Refering to Figure 2, connect one of the input gates (white lead) to "Q".
2. Connect the input of the other gate (white lead) to "$\overline{Q}$".
3. The blue "P" lamp will not be illuminated indicating 180° out-of-phase relationship between "Q" and "$\overline{Q}$".